REMARKS

Claims 1-26 are pending in this application with claims 1, 11, 14, 19, and 23 being independent. Claims 4 and 5 have been amended to place the application in better condition for initial examination. No new matter has been added.

Attached is a marked-up version of the changes being made by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

The examiner is invited to contact the undersigned with any questions at the number set forth below. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the specification:

The paragraph beginning at page 26, line 16 has been amended as follows:

Specifications of the FPC input terminals used in this embodiment are shown in Table 1. Note that the "terminal Nos." in Table 1 correspond to the numbers (1 to 100) above the FPC input portions (1) 904a and the FPC input portions (2) 904b in Fig. 9.

[[Table 1]]

terminal No.	symbol of terminal	voltage (range) [V]	remarks (name of signal etc.)
			pad (dummy terminal)
1	EL_CATH	approximately 4 (0.0~9.0)/9	EL driving direct current power supply (negative terminal)
2	EL_ANOD	9	EL driving direct current power supply (positive terminal)
3	S_LATb	0.0/9.0	latch inversion signal of source driver circuit
4	S_LAT	0.0/9.0	latch signal of source driver circuit
5	VD_16	0.0/9.0	digital video signal 16
6	VD_15	0.0/9.0	digital video signal 15
7	VD_14	0.0/9.0	digital video signal 14
8	VD_13	0.0/9.0	digital video signal 13
9	VD_12	0.0/9.0	digital video signal 12
10	VD_11	0.0/9.0	digital video signal 11
11	VD_10	0.0/9.0	digital video signal 10
12	VD_09	0.0/9.0	digital video signal 9
13	VD_08	0.0/9.0	digital video signal 8
14	VD_07	0.0/9.0	digital video signal 7
15	VD_06	0.0/9.0	digital video signal 6
16	VD_05	0.0/9.0	digital video signal 5
17	VD_04	0.0/9.0	digital video signal 4
18	VD_03	0.0/9.0	digital video signal 3
19	VD_02	0.0/9.0	digital video signal 2
20	VD_01	0.0/9.0	digital video signal 1
21	S_GND	0	negative power supply of source driver circuit
22	S_VDD	9	positive power supply of source driver circuit
23	S_LEFT	0.0 or 9.0	switching of scanning direction of source driver circuit (0.0: scanning to the right, 9.0: scanning to the left)
24	S_SP	0.0/9.0	start pulse of source driver circuit
25	S_CKb	0.0/9.0	inverted clock signal of source driver circuit
26	S_CK	0.0/9.0	clock signal of source driver circuit
27	VD_01	0.0/9.0	digital video signal 1
28	VD_02	0.0/9.0	digital video signal 2
29	VD_03	0.0/9.0	digital video signal 3
30	VD_04	0.0/9.0	digital video signal 4
31	VD_05	0.0/9.0	digital video signal 5
32	VD_06	0.0/9.0	digital video signal 6
33	VD_07	0.0/9.0	digital video signal 7
34	VD_08	0.0/9.0	digital video signal 8
35	VD_09	0.0/9.0	digital video signal 9
36	VD_10	0.0/9.0	digital video signal 10
37	VD_11	0.0/9.0	digital video signal 11
38	VD_12	0.0/9.0	digital video signal 12
39	VD_13	0.0/9.0	digital video signal 13
40	VD_14	0.0/9.0	digital video signal 14
41	VD_15	0.0/9.0	digital video signal 15
42	VD_16	0.0/9.0	digital video signal 16
43	G_GND	0	negative power supply of gate driver circuit
44	G_VDD	10	positive power supply of gate driver circuit
45	G_UP	0.0 or 10.0	switching of scanning direction of gate driver circuit (0.0: scanning to the right, 9.0: scanning to the left)
46	G_CKb	0.0/10.0	inverted clock signal of gate driver circuit
47	G_CK	0.0/10.0	clock signal of gate driver circuit
48	G_SP	0.0/10.0	start pulse of gate driver circuit
49	EL_ANOD	9	EL driving direct current power supply (positive terminal)
50	EL_CATH	approximately 4 (0.0~9.0)/9	EL driving direct current power supply (negative terminal)
			pad (dummy terminal)

The paragraph beginning at page 27, line 10 has been amended as follows:

Table 2 shows the size of TFTs included in the shift register, the NAND circuits, and the buffers which constitute the gate driver circuits of this embodiment. The shift register, the NAND circuits, and the buffers use p-channel TFTs and n-channel TFTs, and both of them are shown in Table 2. The symbols in Table 2 correspond to reference symbols of Fig. 11. L[μm] in Table 2 represents the channel length of the TFT whereas W[μm] represents the channel width of the TFT.

[[Table 2]]

Pch-TFT	L[μm]	W[μm]	Nch-TFT	L[μm]	Lov[μm]	W[μm]
g_chsw_a	4.5	20	g_chsw_a	5	0.5	10
g_sftr_b	4.5	16	g_sftr_b	5	0.5	8
g_sftr_c	4.5	40	g_sftr_c	5	0.5	20
g_sftr_d	4.5	10	g_sftr_d	5	0.5	5
g_nand_e	4.5	22	g_nand_e	5	0.5	22
g_bufff_f	4.5	50	g_buff_f	5	0.5	25

The paragraph beginning at page 28, line 18, has been amended as follows:

Table 3 shows the size of TFTs included in the shift register, the NAND circuits, and the buffers which constitute the source driver circuit of this embodiment. The shift register, the NAND circuits, and the buffers use p-channel TFTs and n-channel TFTs, and both of them are shown in Table 3. The symbols in Table 3 correspond to the reference symbols of Fig. 12. L[μm] in Table 3 represents the channel length of the TFT whereas W[μm] represents the channel width of the TFT. The channel length of the n-channel TFT includes an LOV region.

[[Table 3]]

Pch-TFT	L[μm]	W[μm]	Nch-TFT	L[μm]	Lov[μm]	W[μm]
s_chsw_a	4.5	60	s_chsw_a	5	0.5	40
s_sftr_b	4.5	50	s_sftr_b	5	0.5	25
s_sftr_c	4.5	100	s_sftr_c	5	0.5	50
s_sftr_d	4.5	30	s_sftr_d	5	0.5	15
s_nand_e	4.5	50	s_nand_e	5	0.5	50
s_buf1_f	4.5	100	s_buf1_f	5	0.5	50
s_buf1_g	4.5	100	s_buf1_g	5	0.5	50
s_buf1_h	4.5	300	s_buf1_h	5	0.5	150
s_buf1_i	4.5	400	s_buf1_i	5	0.5	200
s_lat1_j	4.5	16	s_lat1_j	5	0.5	8
s_lat1_k	4.5	16	s_lat1_k	5	0.5	8
s_lat1_m	4.5	4	s_lat1_m	5	0.5	2
s_buf2_n	4.5	30	s_buf2_n	5	0.5	15
s_lat2_p	4.5	16	s_lat2_p	5	0.5	8
s_lat2_r	4.5	16	s_lat2_r	5	0.5	8
s_lat2_s	4.5	4	s_lat2_s	5	0.5	2
s_buf3_t	4.5	30	s_buf3_t	5	0.5	15

The paragraph beginning at page 28, line 23 and continuing to page 29, line 3 has been amended as follows:

Specifications of the display panel according to this embodiment are shown in Table 4.

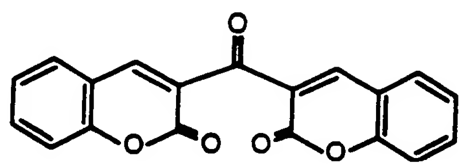
[[Table 4]]

size of screen	diagonal 4.0 inches
number of pixels	640 × 480
interval of pixels	126 μm
grey scales	64 (6bit)
aperture ratio	60%
operating clock frequency of source driver circuit	12. 5MHz
operating clock frequency of gate driver circuit	252kHz
voltage of driver circuit	12V
voltage of display region	6V
duty ratio	61.5%
color	monochrome

The paragraph beginning at page 58, line 20, has been amended as follows:

The molecular formula of the EL material (coumarin pigment) reported in the above article is shown below.

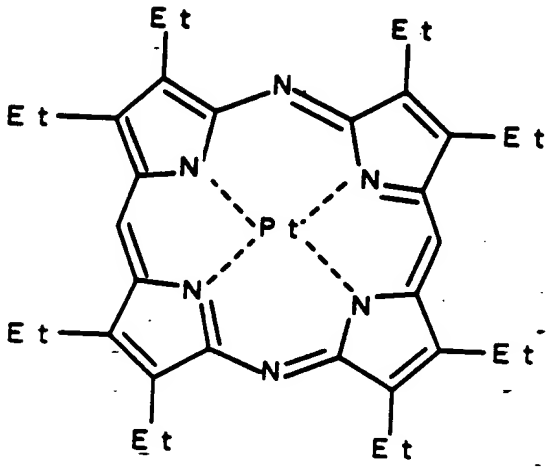
[[Chemical formula 1]]



The paragraph beginning at page 58, line 24, has been amended as follows:

The molecular formula of the EL material (Pt complex) reported in the above article is shown below.

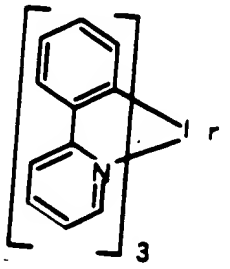
[[Chemical formula 2]]



The paragraph beginning at page 59, line 12, has been amended as follows:

The molecular formula of the EL material (Ir complex) reported in the above article is shown below.

[[Chemical formula 3]]



In the claims:

4. (Amended) A self-luminous device according to **[claim1]** claim 1, wherein the source region and the separate semiconductor film are electrically connected to their respective power supply lines.

5. (Amended) A self-luminous device according to **[claim1]** claim 1, wherein the separate semiconductor film has a region that overlaps with the gate electrode with the gate insulating film sandwiched therebetween, and the region overlapping with the gate electrode takes up 60% or more of the separate semiconductor film.